Amendments To the Abstract of the Disclosure
(Clean Version: Replacement Sheet)

Please replace the Abstract of the Disclosure with the following amended paragraph:

A data input device of a DDR SDRAM includes at least a clock pulse generator (for outputting a data-in-strobe signal based on internal clock), first and second data buffers (being controlled by the data-in-strobe signal and having output lines corresponding to first and second global input-output lines, respectively). When a second control signal is low, the first data is directly applied to the first data buffer for transfer to the first global input/output line, and the second data is directly applied to the second data buffer for transfer to the second global input/output line. When the second control signal is high, the first data is directly applied to the second data buffer for transfer to the second global input/output line, and the second data is directly applied to the first data buffer for transfer to the first global input/output line. The time for the write operation is reduced by directly applying the write-in-strobe signal to the data buffers.